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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,047	04/08/2004	Jente B. Kuang	AUS920040022US1	9651

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EXAMINER	
TAN, VIBOL	
ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 09/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,047	KUANG ET AL.	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Uhlmann (U. S. PAT. 6,211,713).

In claim 1, Uhlmann teaches all claimed features in Fig. 3A, an interface logic circuit for coupling a domain output (Latch_Node) of a first logic circuit domain (not shown, would be a circuit coupling to Latch_Node) to a domain input (Feedback_Node) of a second logic circuit domain (not shown, would be a circuit coupling to Feedback_Node) comprising: a first cut-circuit (308) powered by first and second voltage potentials (inherent, Vcc and ground) and having a first input (306) coupled to the domain output, and a first output (304) coupled to the domain input, wherein the first voltage potential (Vcc) is coupled to the first cut-circuit (308) in response to a first logic state (logic 0) of a first control signal (310) and decoupled from the first cut-circuit in response to a second logic state (logic 1) of the first control signal (312 is 310 inverted); and a latch circuit (302, 314) having a latch input (same as 306) coupled to the first input (306), and a latch output (same as 304) coupled to the first output (304), wherein the latch circuit latches logic states at the domain input (Feedback_Node) when the first voltage potential is decoupled (disconnected) from the first cut circuit.

In claims 2 and 19, Uhlmann further teaches, the interface logic circuit of claim 1, wherein the latch circuit (302, 314) is powered by the second voltage potential (ground) and a third voltage potential (inherent), and the third potential is coupled to the latch circuit in response to the first logic state (logic 0) of a second control signal (316) and decoupled from the latch circuit in response to the second logic state (logic 1) of the second control signal; and wherein the first and third voltage potentials are equal (inherent).

In claims 3 and 4, Uhlmann further teaches, the interface logic circuit of claim 2, wherein the second voltage potential (ground) is coupled to the first cut-circuit (308) in response to the second logic state (logic 1) of the second control signal (316) and decoupled from the first cut-circuit in response to the first logic state of the second control signal; and wherein the second voltage potential (ground) is coupled to the latch circuit (302, 314) in response to the second logic state (logic 1) of the second control signal and decoupled from the latch circuit in response to the first logic state (logic 0) of the second control signal.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uhlmann in view of Taguchi et al. (U. S. PAT. 5,557,221).

In claim 5, Uhlmann teaches, the interface logic circuit of claim 1, with the exception of teaching wherein the first cut-circuit comprises: an inverter stage having an inverter input coupled as the input of the first cut-inverter, an inverter output coupled as the output of the first cut-inverter, a first power supply node, and a second power supply node coupled to the second voltage potential. However, Taguchi et al. teaches in Fig. 1, the first cut-circuit (36-39) comprises: an inverter stage (36, 37) having an inverter input (as shown) coupled as the input of the first cut-inverter, an inverter output coupled as the output of the first cut-inverter (as shown), a first power supply node (Vcc), and a second power supply node coupled to the second voltage potential (ground); and a first electronic switch (38) coupling the first voltage potential to the first power supply node in response to the first logic state (logic 0) of the first control signal and decoupling the first voltage potential from the first power supply node in response to the second logic state (logic 1) of the first control signal.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of Uhlmann with the teachings of Taguchi et al. in order to provide an interface logic circuit which operates in an electrical stable manner, and when in normal operation it operates at a high speed and low power consumption.

In claims 6 and 7, Taguchi further teaches the interface circuit of claim 5, wherein the latch circuit (35) comprises: a first inverter (43, 44) having a first inverter input as the latch input and a first inverter output as the latch output (as shown); and a second cut-inverter (41, 42) having an input coupled to the latch output, an output coupled to the

latch input, wherein the second voltage potential (ground) is coupled to the second cut-inverter in response to the second logic state (logic 1) of a first control signal (CONT SGL) and decoupled from the second cut-inverter in response to the first logic state (logic 1) of the first control signal; and further comprising a second electronic switch (46) coupling the second voltage potential (Vss or ground) to the second power supply node in response to the second logic state (logic 1) of a second control signal (inverse of the first signal) and decoupling the second voltage potential from the second power supply node in response to the first logic state of the second control signal.

Claims 8-18 correspond to detailed circuitry already discussed similarly with regard to claims 5-7.

5. Claims 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tobin et al. (U. S. PAT. 6,275,077) in view of Uhlmann.

In claim 20, Tobin et al. teaches all claimed features in Fig. 15, a data processing system comprising: a central processing unit (1502); a random access memory (1504); an input output (1506) interface unit; and a bus (not labeled) for coupling the CPU, RAM and I/O interface unit, the CPU having first and second logic circuit domains (inside 1502) and an interface logic circuit (1508) for coupling a domain output from the first logic circuit domain to a domain input to the second logic circuit domain; with the exception of teaching the details of the interface circuit. However, Uhlman teaches in Fig. 3A, an interface logic circuit for coupling a domain output (Latch_Node) of a first logic circuit domain (not shown, would be a circuit coupling to Latch_Node) to a domain input (Feedback_Node) of a second logic circuit domain (not shown, would be a circuit

coupling to Feedback_Node) comprising: a first cut-circuit (308) powered by first and second voltage potentials (inherent, Vcc and ground) and having a first input (306) coupled to the domain output, and a first output (304) coupled to the domain input, wherein the first voltage potential (Vcc) is coupled to the first cut-circuit (308) in response to a first logic state (logic 0) of a first control signal (310) and decoupled from the first cut-circuit in response to a second logic state (logic 1) of the first control signal (312 is 310 inverted); and a latch circuit (302, 314) having a latch input (same as 306) coupled to the first input (306), and a latch output (same as 304) coupled to the first output (304), wherein the latch circuit latches logic states at the domain input (Feedback_Node) when the first voltage potential is decoupled (disconnected) from the first cut circuit.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teaching of Tobin et al. with the teachings of Uhlmann in order to provide an interface logic circuit having a controllable feedback source for a CMOS latch that operates in an electrical stable manner, and when in normal operation it operates at a high speed and low power consumption for a data processing system.

In claims 21 and 24, Uhlmann further teaches, the data processing system of claim 20, wherein the latch circuit (302, 314) is powered by the second voltage potential (ground) and a third voltage potential (inherent), and the third potential is coupled to the latch circuit in response to the first logic state (logic 0) of a second control signal (316) and decoupled from the latch circuit in response to the second logic state (logic 1) of the

second control signal; and wherein the first and third voltage potentials are equal (inherent).

In claims 22 and 23, Uhlmann further teaches, the data processing system of claim 21, wherein the second voltage potential (ground) is coupled to the first cut-circuit (308) in response to the second logic state (logic 1) of the second control signal (316) and decoupled from the first cut-circuit in response to the first logic state of the second control signal; and wherein the second voltage potential (ground) is coupled to the latch circuit (302, 314) in response to the second logic state (logic 1) of the second control signal and decoupled from the latch circuit in response to the first logic state (logic 0) of the second control signal.

Response to Arguments

6. Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection.

The new ground of rejection(s) set forth, as discussed in detail above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VIBOL TAN
PRIMARY EXAMINER